REMARKS

The Final Office Action mailed June 2, 2005, has been received and reviewed. Claims 1 through 9 and 12 through 19 are currently pending in the application. Claims 1 through 9 and 12 through 19 stand rejected. Applicants propose to amend no claims, and respectfully request reconsideration of the application as proposed herein.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,427,194 to Owen et al. in view of U.S. Patent 5,469,208 to Dea and further in view of U.S. Patent No. 6,040,845 to Melo et al.

Claims 1 through 3, 5 through 9 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Owen et al. (U.S. Patent No. 6,427,194) in view of Dea (U.S. Patent No. 5,469,208) and further in view of Melo et al. (U.S. Patent No. 6,040,845). Applicants respectfully traverse this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
>
> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 1 through 3, 5 through 9, and 12 are improper because the elements for a *prima facie* case of obviousness are not met to establish a *prima facie* case of obviousness regarding the presently claimed invention. Specifically, the rejection of the presently claimed invention fails to meet the criterion that the prior art references must teach or suggest all the claim limitations and the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure, to establish a *prima facie* case of obviousness.

Specifically, Applicants' independent claim 1 recites:

> 1. A method for compressing video data in a computer system comprising:
>
> ***receiving a current video frame at a dedicated video input*** of a core logic chip in the computer system ***directly from a video source originating the video frame***, the computer system including the core logic chip for directly coupling a processor to a system memory and for coupling the processor and the system memory to a system bus;
>
> ***computing*** at the core logic chip ***a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input*** of the core logic chip, the previous video frame being received at the core logic chip as a previous current video frame and retained therein, the difference frame including computing the difference frame in the core logic chip within the computer system, wherein the core logic chip is a north bridge chip;
>
> ***storing the difference frame directly*** from the core logic chip to the system memory in the computer system ***via a dedicated memory interface*** therebetween; and
>
> the processor retrieving the difference frame directly from the system memory via the core logic chip using a dedicated processor interface therebetween to complete compression of the video data. (Emphasis added.)

The Office Action alleges in the Response to Arguments:

> Dea discloses in col. 9, lines 60-63 that "The encoding pathway receives a previous image and a current image into buffers 204, 206 respectively. The difference between the two may be applied by frame difference block 220 to selectable discrete cosine transform block 230". It is noted that previous image is current image delayed by one image. ***Thus, the claimed "receiving a current video frame at a dedicated video input of a core logic chip ... directly from a video source originating the video frame ..." is anticipated by buffer 206 of Dea and the claimed "computing*** at the core logic chip ***a difference*** from the current video frame and a previous video frame ***as the current video frame streams into the dedicate video input*** of the core logic chip, the previous video frame being received at the core logic chip as a previous current video frame and retained therein, ..." ***is anticipated by frame different block 220 of Dea*** because the previous image is the current image delay by one image. (Office Action, pp. 2-3.; emphasis added).

Applicants respectfully disagree with the characterization of the teachings of Dea and Owen. Applicants' computing of a difference frame is performed in a pipelined configuration, specifically via a receiving input, namely the "dedicated video input" and a storing output,

namely "a dedicated memory interface." Specifically, Applicants' invention as claimed in independent claim 1 is drawn to "***receiving a current video frame at a dedicated video input*** ... ***directly from a video source originating the video frame***, ...; ***computing*** ... ***a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input*** ...; ***storing the difference frame directly*** ... ***via a dedicated memory interface*** ...."

In contrast, in the ***Owen reference***, any computing of a difference frame would need to occur in decoder/encoder 80 (FIG. 3) which is isolated by a ***single interface***, namely memory bus 167 (FIG. 3). Similarly and also in contrast to Applicants' invention as claimed, in the ***Dea reference*** teaches or suggests a compression/decompression accelerator 120 which includes a frame difference block 220 for calculating a difference frame from current frame memory 204 and previous frame memory 206 wherein "[a]ll RAM within accelerator 120 must read and write by way of accelerator bus interface 200."(Col. 5, lines 40-42). Such an architecture is clearly visible with reference to FIGS. 1 and 2 where the frame difference block 220 is only accessible by way of a ***single interface*** 200 which retrieves the values from the current frame memory 204 and the previous frame memory 206 which where previously stored there. Therefore, the frame difference block 220 of Dea can only be fed frame data for calculating a difference frame from data that has been stored and retrieved from memory 114.

The Office Action cites Melo et al for "teach[ing] that using conventional master/slave nomenclature, the graphics accelerator can be considered an AGP compliant master, the north bridge, and specifically, the memory controller or core logic within the north bridge can be partially considered as an AGP compliant target . . ." (Office Action, p. 5.), which does not provide any further teaching or suggestion for the claim limitations as previously stated.

Therefore, since neither Owen, Dea, nor Melo, individually or in any proper combination, teach or suggest "***receiving a current video frame at a dedicated video input*** ... ***directly from a video source originating the video frame***, ...; ***computing*** ... ***a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input*** ...; ***storing the difference frame directly*** ... ***via a dedicated memory***

interface" as claimed by Applicants, any combination of the cited references cannot render obvious Applicants' invention as presently claimed.

Applicants submit that since none of the references, nor any combination thereof, teach, suggest or motivate Applicants' invention as claimed in independent claim 1, the rejection should be withdrawn and claims 1 through 3, 5 through 9, and 12 passed to allowance.

Obviousness Rejection Based on U.S. Patent No. 6,427,194 to Owen et al. in view of U.S. Patent No. 5,469,208 to Dea, U.S. Patent No. 6,040,845 to Melo et al., and further in view of U.S. Patent No. 4,546,383 to Abramatic et al.

Claims 4 and 13 through 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Owen et al. (U.S. Patent No. 6,427,194) in view of Dea (U.S. Patent No. 6,040,845), Melo et al. (U.S. Patent No. 6,040,845), and further in view of Abramatic et al. (U.S. Patent No. 4,546,383). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 4 and 13 through 19 are improper because the elements for a *prima facie* case of obviousness are not met to establish a *prima facie* case of obviousness regarding the presently claimed invention. Specifically, the rejection of the presently claimed invention fails to meet the criterion that the prior art references must teach or suggest all the claim limitations and the teaching or suggestion to make the

claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure, to establish a *prima facie* case of obviousness.

Regarding claim 4, Applicants respectfully assert that claim 4 depends from independent claim 1 and reassert the above proffered arguments in support of the allowability of independent claim 1. Applicants request the rejection of claim 4 be withdrawn based at least on its dependency on independent claim 1.

Regarding independent claim 13, from which dependent claims 14 through 19 depend, Applicants' independent claim 13 recites:

> 13. A method for compressing video data in a computer system, comprising:
> ***receiving a current video frame at a dedicated video input*** of a core logic chip in the computer system ***directly from a video source originating the video frame***, the computer system including the core logic chip for directly coupling a processor to a system memory and for coupling the processor and the system memory to a system bus;
> ***computing*** at the core logic chip ***a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input*** of the core logic chip, the previous video frame being received at the core logic chip as a previous current video frame and retained therein, the difference frame including computing an exclusive-OR between the current video frame and the previous video frame, and wherein computing the difference frame includes computing the difference frame in the core logic chip within the computer system, wherein the core logic chip is a north bridge chip;
> ***storing the difference frame directly*** from the core logic chip into the system memory in the computer system ***via a dedicated memory interface*** therebetween;
> storing the current video frame directly from the core logic chip into the system memory in the computer system using a dedicated processor interface therebetween;
> the processor retrieving the difference frame directly from the system memory via the core logic chip; and
> compressing the video data using the difference frame to produce compressed video data. (Emphasis added.)

Again, the Office Action alleges in the Response to Arguments:

Dea discloses in col. 9, lines 60-63 that "The encoding pathway receives a previous image and a current image into buffers 204, 206 respectively. The difference between the two may be applied by frame difference block 220 to selectable discrete cosine transform

> block 230". It is noted that previous image is current image delayed by one image. ***Thus, the claimed "receiving a current video frame at a dedicated video input of a core logic chip ... directly from a video source originating the video frame ..." is anticipated by buffer 206 of Dea and the claimed "computing*** at the core logic chip ***a difference*** from the current video frame and a previous video frame ***as the current video frame streams into the dedicate video input*** of the core logic chip, the previous video frame being received at the core logic chip as a previous current video frame and retained therein, ..." ***is anticipated by frame different block 220 of Dea*** because the previous image is the current image delay by one image. (Office Action, pp. 2-3.; emphasis added).

Again, Applicants respectfully disagree with the characterization of the teachings of Dea and Owen. Applicants' computing of a difference frame is performed in a pipelined configuration, specifically via a receiving input, namely the "dedicated video input" and a storing output, namely "a dedicated memory interface." Specifically, Applicants' invention as claimed in independent claim 13 is drawn to "***receiving a current video frame at a dedicated video input ... directly from a video source originating the video frame***, ...; ***computing ... a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input*** ...; ***storing the difference frame directly ... via a dedicated memory interface*** ...."

Again and in contrast, in the ***Owen reference***, any computing of a difference frame would need to occur in decoder/encoder 80 (FIG. 3) which is isolated by a ***single interface***, namely memory bus 167 (FIG. 3). Similarly and also in contrast to Applicants' invention as claimed, in the ***Dea reference*** teaches or suggests a compression/decompression accelerator 120 which includes a frame difference block 220 for calculating a difference frame from current frame memory 204 and previous frame memory 206 wherein "[a]ll RAM within accelerator 120 must read and write by way of accelerator bus interface 200."(Col. 5, lines 40-42). Such an architecture is clearly visible with reference to FIGS. 1 and 2 where the frame difference block 220 is only accessible by way of a ***single interface*** 200 which retrieves the values from the current frame memory 204 and the previous frame memory 206 which where previously stored there. Therefore, the frame difference block 220 of Dea can only be fed frame data for calculating a difference frame from data that has been stored and retrieved from memory 114.

The Office Action cites Melo et al for "teach[ing] that using conventional master/slave nomenclature, the graphics accelerator can be considered an AGP compliant master, the north bridge, and specifically, the memory controller or core logic within the north bridge can be partially considered as an AGP compliant target . . ." (Office Action, p. 5.), which does not provide any further teaching or suggestion for the claim limitations as previously stated.

The Office Action cites Abramatic for "disclos[ing] the claied step of computing an exclusieve-OR between the current video frame ad the previous video frame . . .." (Office Action, p. 11).

Therefore, since neither Owen, Dea, Melo, nor Abramatic nor any combination thereof, teach or suggest "***receiving a current video frame at a dedicated video input*** ... ***directly from a video source originating the video frame***, ...; ***computing*** ... ***a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input*** ...; ***storing the difference frame directly*** ... ***via a dedicated memory interface***" as claimed by Applicants, the cited references cannot render obvious Applicants' invention as presently claimed.

Applicants submit that since none of the references nor any combination thereof, teach, suggest or motivate Applicants' invention as claimed in independent claim 13, the rejection should be withdrawn and claims 13 through 19 passed to allowance.

ENTRY OF AMENDMENT

No amendments to the claims are proposed herein and hence do not raise any new issues that could require a further search. Finally, if the Examiner determines that the remarks do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 1 through 9 and 12 through 19 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,

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Date: August 2, 2005
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